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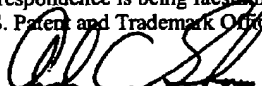
Title:	INTEGRATED CIRCUIT INCORPORATING THREE-DIMENSIONAL MEMORY ARRAY WITH DUAL OPPOSING DECODER ARRANGEMENT		
Application No.:	10/774,818	Filed:	February 9, 2004
Examiner:	Unknown	Group Art Unit:	2812
Atty. Docket No.:	023-0025	Confirmation No.:	9232

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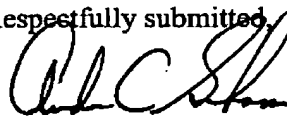
- (1) Information Disclosure Statement (2 pages)
- (2) Form(s) PTO/1449 (7 pages), with copy of no references;
- (3) Form(s) PTO/SB/08A (1 page), with copy of no references.

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Andrew C. Graham 2-23-05
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Respectfully submitted,



Andrew C. Graham, Reg. No. 36,531
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PATENT

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant(s): Mark G. Johnson et al.

Title: INTEGRATED CIRCUIT INCORPORATING THREE-DIMENSIONAL
MEMORY ARRAY WITH DUAL OPPOSING DECODER
ARRANGEMENT

Application No.: 10/774,818

Filed: February 9, 2004

Examiner: Unknown

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February 23, 2005

Mail Stop Amendment
COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, VA 22313-1450**INFORMATION DISCLOSURE STATEMENT**
37 C.F.R. § 1.97(b)

Dear Sir:

Pursuant to 37 C.F.R. § 1.56, § 1.97 and § 1.98, the undersigned brings to the Examiner's attention in the above-identified application the patents, publications, applications or other information identified in the attached:

- ☒ Form(s) PTO/1449 (7 page(s), with copy of no reference(s)).
- ☒ Form(s) PTO/SB/08A (1 page(s), with copy of no reference(s)).
- ☐ Form(s) PTO/SB/08B (N/A page(s), with copy of no reference(s)).
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- ☐ Other: N/A

Citation of such information shall not be construed as (i) an admission that the information necessarily is, or corresponds to, prior art with respect to the instant invention, (ii) a representation that a search has been made, other than as described herein, or (iii) an admission that the information cited herein is, or is considered to be, material to patentability as defined in § 1.56(b).

For each item of information listed that is not in the English language, the undersigned has provided a concise explanation of the relevance through (i) an English language abstract, (ii) an English language equivalent application, or (iii) if cited in a search report or other action by a foreign patent office in a counterpart foreign application, an English language version of the search report or action that indicates the degree of relevance found by the foreign office.

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Pursuant to operative regulations, certain copies need not be provided and corresponding information is identified in this Information Disclosure Statement by citation only. In particular,

- ☒ In accordance with 37 C.F.R. § 1.98(a)(2)(ii), copies of cited U.S. Patents and U.S. Patent Application Publications are not included.
- ☒ Certain information was submitted to, or cited by, the Office in Application No(s). 10/253,354 and 09/939,431, filed September 23, 2002 and August 24, 2001, respectively, to which the above-identified application claims priority under 35 U.S.C. § 120. In accordance with 37 C.F.R. § 1.98(d), copies of that information are not included.
- ☐ Pursuant to 1287 OG 163 (October 19, 2004), for those cited pending U.S. patent applications filed (or which entered the national stage under 35 U.S.C. § 371) on or after June 30, 2003 or which are otherwise stored in the USPTO's Image File Wrapper system, copies are not included.

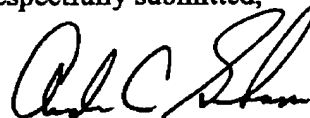
FEE AUTHORIZATION

- ☐ This Information Disclosure Statement is filed within three months of the filing date of a national application other than a continued prosecution application under § 1.53(d) or within three months of entry of the national stage as set forth in § 1.491 in an international application. Therefore, no fee is required.
- ☒ The undersigned believes that this Information Disclosure Statement is being filed before the mailing date of a first Office action on the merits or before the mailing date of a first Office action after the filing of a request for continued examination under § 1.114. Therefore, no fee is believed required.

If however, this Information Disclosure Statement is filed after the period specified in § 1.97(b), the undersigned hereby authorizes the Commissioner to charge the fee set forth in § 1.17(p) to Deposit Account No. 50-0631.

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Andrew C. Graham	Date

Respectfully submitted,



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FORM PTO-1449	SERIAL NO. 10/774,818	ATTY. DOCKET NO. 023-0025
LIST OF PATENTS AND PUBLICATIONS FOR APPLICANT'S INFORMATION DISCLOSURE STATEMENT	FILING DATE February 9, 2004	GROUP ART UNIT 2812
(use several sheets if necessary)		APPLICANT(S): JOHNSON ET AL.

REFERENCE DESIGNATION U.S. PATENT DOCUMENTS

EXAMINER INITIAL		DOCUMENT NUMBER	DATE	NAME	CLASS/ SUBCLASS	FILING DATE
	A1	3,414,892	12/03/1968	MCCORMACK ET AL.		
	A2	3,432,827	03/11/1969	SARNO		
	A3	3,576,549	04/27/1971	HESS ET AL.		
	A4	3,582,908	06/01/1971	KOO		
	A5	3,634,929	01/18/1972	YOSHIDA ET AL.		
	A6	3,717,852	02/20/1973	ABBAS ET AL.		
	A7	3,728,695	04/17/1973	FROHMAN-BENTCHKOWSKY ET AL.		
	A8	3,787,822	01/22/1974	RIOULT		
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	A18	4,507,757	03/26/1985	MCELROY		
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	A35	5,160,987	11/03/1992	PRICER ET AL.		
	A36	5,191,405	03/02/1993	TOMITA ET AL.		
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A108	5,960,539	10/99	BURNS		
A109	5,978,258	11/99	MANNING		
A110	6,049,123	4/00	BURNS		
A111	3,863,231	1/75	TAYLOR		
A112	4,229,757	10/80	MOUSSIE		
A113	5,103,422	4/92	TOKITA ET AL.		

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	A114	4,855,953	8/89	TSUKAMOTO ET AL.		
	A115	5,436,861	7/95	KATTI ET AL.		
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	A119	4,489,478	12/25/1984	SAKURA		
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	A132	5,929,478	7/27/1999	PARRIS ET AL.		
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EXAMINER INITIAL		DOCUMENT NUMBER	DATE	COUNTRY	CLASS/ SUBCLASS	TRANSLATION YES NO
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	A136	JP 60-22352 A	02/04/1985	Japan		Abstract
	A137	JP 61222216 A	10/02/1986	Japan		Abstract
	A138	JP 63-52483 A	03/05/1988	Japan		Abstract
	A139	EP 0 387 834 A2	08/19/1990	Europe		X
	A140	EP 0 395 886 A2	11/07/1990	Europe		X
	A141	EP 0 516 886 A1	12/09/1992	Europe		X
	A142	EP 0 606 653 A1	07/20/1994	Europe		X
	A143	WO 94/26083	11/10/1994	WIPO		X

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	A144	EP 0 644 548 A2	03/22/1995	Europe	X
	A145	EP 0 516 866 A1	12/09/1992	Europe	X
	A146	WO 99/14763	3/25/1999	WIPO	

EXAMINER INITIAL	OTHER ART (Including Author, Title, Date, Pertinent Pages, etc.)	
	A147	Akasaka, Yoichi, "Three-Dimensional Integrated Circuit: Technology and Application Prospect," Microelectronics Journal, Vol. 20 No. 1 - 2, 1989, pages 105 - 111
	A148	Akasaka, Yoichi, "Three-Dimensional IC Trends," Proceedings of the IEEE, Vol. 74, No. 12, December 1986, pages 1703 - 1714
	A149	Bertin, Claude L., "Evaluation of a Three-Dimensional Memory Cube System," IEEE Transactions on Components, Hybrids, and Manufacturing Technology, Vol. 16, No. 8, December 1993, 1006 - 1011
	A150	Camperl-Ginestet, C., "Vertical Electrical Interconnection of Compound Semiconductor Thin-Film Devices to Underlying Silicon Circuitry," IEEE Photonics Technology Letters, Vol. 4, No. 9, September 1992, pages 1003 - 1006
	A151	Frohman-Bentchkowsky, Dov, "A Fully Decoded 2048-Bit Electrically Programmable FAMOS Read-Only Memory," IEEE Journal of Solid-State Circuits, Vol. SC-6, No. 5, October 1971, pages 301 - 306
	A152	Hayashi, Y., "A New Three Dimensional IC Fabrication Technology, Stacking Thin Film Dual-CMOS Layers," IEDM 1991, pages 657 - 660
	A153	Hayasky, Fumihiko, "A Self-Aligned Split-Gate Flash EEPROM Cell with 3-D Pillar Structure" 1999 Symposium on VLSI Technology Digest of Technical Papers, pages 87 - 88
	A154	"3-D Chip-on-Chip Stacking," Industry News, Semiconductor International, December 1991
	A155	Inoue, Y., "A Three-Dimensional Static RAM," IEEE Electron Device Letters, Vol. EDL-7, No. 5, May 1986, pages 327 - 329
	A156	Jokerst, N.M., "Manufacturable Multi-Material Integration Compound Semiconductor," SPIE - The International Society for Optical Engineering, Vol. 2524, July 11 - 12, 1995, pages 152 - 163
	A157	Kurokawa, Takakazu, "3-D VLSI Technology in Japan and an Example: A Syndrome Decoder for Double Error Correction," Future Generations Computer Systems 4, No. 2, September 1988, pages 145 - 155
	A158	Lay, Richard W., "TRW Develops Wireless Multiboard Interconnect System," Electronic Engineering Times, November 5, 1984
	A159	Mallinak, David, "Memory-Chip Stacks Send Density Skyward," Electronic Design 42, No. 17, August 22, 1994, pages 69 - 75
	A160	Pein, Howard, et al., "Performance of the 3-D PENCIL Flash EPROM Cell and Memory Array," IEEE Transactions on Electron Devices, Vol. 42, No. 11, November 1995, pages 1982 - 1991

EXAMINER	DATE CONSIDERED
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EXAMINER INITIAL	OTHER ART (Including Author, Title, Date, Pertinent Pages, etc.)	
	A161	Reber, M., et al., "Benefits of Vertically Stacked Integrated Circuits for Sequential Logic" IEEE 1996, pages 121 - 124
	A162	Sakamoto, Koji, "Architecture of Three Dimensional Devices," Bulletin of The Electrotechnical Laboratory, Vol. 51, No. 1, 1987, pages 16 - 29
	A163	Sato, Noriaki, et al., "A New Programmable Cell Utilizing Insulator Breakdown," IEAM Technical Digest, 1985, pages 639 - 642
	A164	Schlaeppl, H.P., "Microsecond Core Memories Using Multiple Coincidence," 1960 International Solid-State Circuits Conference, Digest of Technical Papers, February 11, 1960, pages 54 - 55
	A165	Schlaeppl, H.P., "Microsecond Core Memories Using Multiple Coincidence," IRE Transactions on Electronic Computers, June, 1960, pages 192 - 198
	A166	Stacked Memory Modules, IBM Technical Disclosure Bulletin, May 1995, pages 433 - 434
	A167	Stern, Jon M., "Design and Evaluation of an Epoxy Three-Dimensional Multichip Module," IEEE Transactions on Components, Packaging, and Manufacturing Technology - Part B, Vol. 19, No. 1, February 1996, pages 188 - 194
	A168	Terrill, Rob, "3D Packaging Technology Overview and Mass Memory Applications," IEEE 1996, pages 347 - 355
	A169	Thakur, Shashidhar, "An Optimal Layer Assignment Algorithm for Minimizing Crosstalk for Three Layer VH V Channel Routing," IEEE 1995, pages 207 - 210
	A170	Watanabe, H., "Stacked Capacitor Cells for High-Density Dynamic RAMs," IEDM 1988, pages 600 - 603
	A171	Yamazaki, K., "Fabrication Technologies For Dual 4-KBIT stacked SRAM," IEDM 1986, pages 435 - 438
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Page 7 of 7

FORM PTO-1449	SERIAL NO. 10/774,818	ATTY. DOCKET NO. 023-0025
LIST OF PATENTS AND PUBLICATIONS FOR APPLICANT'S INFORMATION DISCLOSURE STATEMENT (use several sheets if necessary)	FILING DATE February 9, 2004	GROUP ART UNIT 2812
APPLICANT(S): JOHNSON ET AL.		

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	A182	"Special Report: Memory Market Startups Cubic Memory: 3D Space Savers," Semiconductor Industry & Business Survey, v18, n13, pN/A September 12, 1994
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PTO/SB/08A (Substitute for form 1449/PTO)				Attorney Docket No.: 023-0025		
				Application No.: 10/774,818		
INFORMATION DISCLOSURE STATEMENT BY APPLICANT				First Named Inventor: Mark G. Johnson		
(Use several sheets if necessary)				Filing Date: February 9, 2004		
				Group Art Unit: 2812		
				Examiner Name: Unknown		
				Date Submitted: February 23, 2005		
U.S. PATENT DOCUMENTS						
Examiner Initials*	Cite No. ¹	Document Number Number-Kind Code ² (if known)	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear	
		US-4,442,507	04/1984	Roesner		
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Examiner Initials*	Cite No. ¹	Foreign Patent Document Country Code ³ -Number ⁴ -Kind Code ⁵ (if known)	Publication Date MM-DD-YYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages Or Relevant Figures Appear	T ⁶
		EP 0 800 137 A1	10-1997	Genduso		
Examiner Signature			Date Considered			

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